Design of an FPGA based visible light communication system

Yinjie Jia, Minglun Zhang, Yongqing Huang, Yangan Zhang
State Key Laboratory of Information Photonics and Optical Communications
Beijing University of Posts and Telecommunications
Beijing, 100876, China
{jiayinjie, zhangml, yqhuang, zhang}@bupt.edu.cn

***Abstract*—Visible light communication (VLC) has won much attention in recent years. In this work a visible light communication system based on IEEE 802.3 standard Media Access Control (MAC) layer is presented. The digital signal processing module of the physical (PHY) layer is implemented in FPGA (Field Programmable Gate Array). The PHY layer is connected to the MAC layer via a Media Independent Interface (MII) which has been specified in IEEE 802.3 standard. The digital part of the system is tested by a Streaming Media Server system. Maximum data rate of 30 Mb/s is achieved.**

Keywords—visible light communication, wireless optical communication, optical networks

I. INTRODUCTION

In recent years, light-emitting diode (LED) has been considered as the most promising lighting device for the future lighting technology. On the other hand, LEDs of high modulation rate and shot response time are used for wireless optical communication. Feasibility and fundamental principles of this technique have been analyzed in [1]. In a VLC system, LED can be used for illumination and communication at the same time. Compared with conventional RF communication, VLC has many attractive features such as occupying no RF spectrum, unlicensed bandwidth, immunity to electromagnetic interference and low energy cost.

Along with the development of research on modulation and equalization technology, data rates of VLC systems have been greatly improved. Applications of VLC, such as indoor broadband accessing, indoor positioning and outdoor traffic information transmission have been researched [2, 3]. In 2009, a PHY and MAC standard for VLC has been completed by the IEEE 802.15.7 VLC Task Group. Though many experiments and simulations related to this standard have been done, the research on VLC is still in laboratory stage.

At present, most researches on VLC focus on achieving higher data rate transceiver circuit by using different methods. Design and implementation of higher layer of VLC system received little attention. In this paper, our work aims to design and implement a higher layer used to control the transceiver circuit in a VLC system. Proceeding from this angle, a VLC system is designed and its higher layer is implemented. An IEEE 802.3 standard MAC layer is adopted. Digital module of the PHY layer is implemented in FPGA. IP traffic is supported by the system.

II. PROPOSED SYSTEM

Our VLC system is designed to perform peer-to-peer and bidirectional communication. The connection can realize full-duplex communication between two computers. Block diagram of a terminal that performs the function of communication is shown in figure 1.

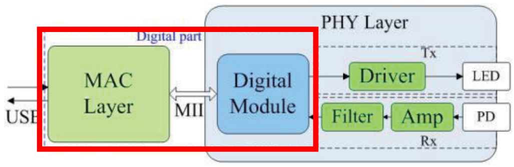

Fig. 1. Block diagram of a terminal

The VLC terminal is connected to a computer through a USB port. In order to ensure the robustness of the system, the terminal is divided into two layers: Media Access Control (MAC) layer and physical (PHY) layer. This hierarchy also makes it easy for the future expansions and upgrades of the prototype system.

The MAC layer of the terminal is based on CSMA/CD protocol. In our VLC system, since there is no collision in peer-to-peer communication, the MAC layer can be configured to work in full-duplex mode. The PHY layer of the terminal comprises a digital module and necessary transceiver circuit. Data exchange between the MAC layer and the PHY layer is realized by a Media Independent Interface (MII), which has been specified in IEEE 802.3 standard.

At the transmitting side, data stream from MAC layer is firstly processed by the digital module of PHY layer. This processing procedure includes 4B/5B encoding, Manchester encoding and generating proper preamble for synchronization and clock recovery at the receiver. Then the digital signal is used as input of the driver circuit to control the LED to emit visible light.

At the receiving side, weak light is received by a photodetector. Generally, the photocurrent signal is very weak, so trans-impedance amplifier and filter are used to amplify the signal and suppress noise. Then the received signal is input

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into the digital module for data recovery, synchronization and decoding. Finally, the recovered data frame is sent to the MAC layer through the MII interface.

III. DESCRIPTION OF THE DIGITAL PART

In this work, we mainly focus on the implementation of the digital part that controls the transceiver circuit in a VLC system. The digital part of the system comprises a MAC layer and a digital module of the PHY layer as shown in figure 1.

A. MAC Layer

Taking into consideration of simplicity, a CSMA/CD protocol based MAC layer is adopted. This MAC layer has been used in Ethernet and proved to be suitable to carry IP traffic and easy to be managed. In our work, a USB to Ethernet controller chip is used as MAC layer of the terminal. This Ethernet controller chip comprises an IEEE 802.3 standard MAC layer, a USB controller and a MII interface. The MAC layer is configured to work in full-duplex mode.

B. Digital module of the PHY Layer

The PHY layer consists of a digital module and necessary transceiver circuit. In our system, the digital module is implemented in FPGA. Figure 2 depicts a schematic view of the digital module. For the sake of clarity, some signals are omitted.

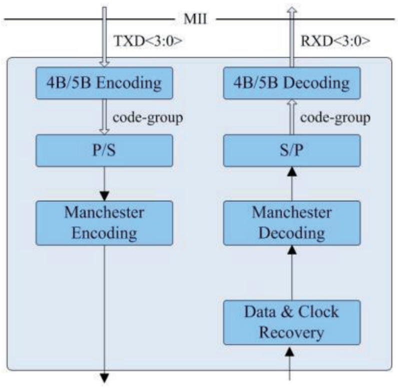

Fig. 2. Diagram of the digital module

At the transmitting side, four-bit nibbles from MII interface are mapped into five-bit code-groups using a 4B/5B encoding scheme. Code-groups are then converted to a serial bit stream and Manchester encoded. At the receiving side, a reverse processing is performed after data and clock recovery.

Here, the main purpose of using 4B/5B encoding scheme is to insert control code-groups in the data stream. This coding scheme has been specified in IEEE 802.3 standard. Control code-groups, such as Start-of-Stream delimiter (SSD) and End-of-Stream delimiter (ESD), can be used at the receiving side to indicate start or end of valid data stream and establish code-group boundaries.

In order to make it easy for the receiver to recover data and clock, Manchester code is used as line code. In Manchester encoding, each data bit has at least one transition and the DC component of the encoded signal is not dependent on the data. These advantages help clock recovery and eliminate baseline wander at the receiver. Moreover, in VLC system, the Manchester encoding scheme can eliminate flicker of light because of the constant average power of the encoded signal.

A data and clock recovery module is implemented at the receiving side to recover data and clock from the received signal. The digital module we implemented can recover data and clock of a received signal whose bit rate up to 100Mb/s.

IV. EXPERIMENTAL RESULTS

Experiments of the digital part is performed. A commercial MAC layer demo board is used. The digital module of the PHY layer is implemented in FPGA Virtex5. Waveform of the received signal, recovered data and recovered clock are shown in figure 3.

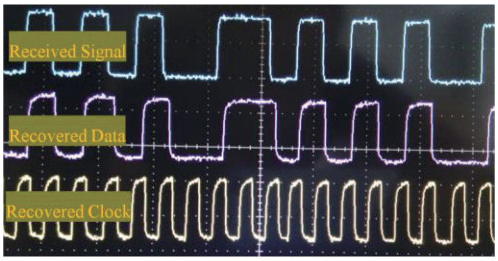

Fig. 3. Waveform of received signal, recovered data and recovered clock

A Streaming Media Server is setup to test the system. The client computer can access the server through the link. Real-time video can be transmitted. The maximum data rate of 30Mb/s (at the IP layer) is achieved.

V. CONCLUSION

In this paper a VLC system based on FPGA is presented. The system is intended to support IP traffic between two computers. An IEEE 802.3 standard MAC Layer is adopted. 4B/5B encoding and Manchester encoding are used to improve the robustness of the system. The digital signal processing of the PHY layer is implemented in FPGA. A Streaming Media Server is setup to test the digital part of the system. Data rate of 30Mb/s is achieved.

ACKNOWLEDGMENT

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REFERENCES

[1] T. Komine, M. Nakagawa, “Fundamental analysis for visible light communications using LED lights,” IEEE transactions on Consumer Electronics, Vol. 50, Number 1, pp. 100-107, February 2004.

[2] F. Delgado, I. Quintana, J. Rufo, J. A. Rabadan, C. Quintana and R. Perez-Jimenez, “Design and implementation of an Ethernet-VLC interface for broadcast transmissions,” IEEE Commun. Lett., vol.14, no.12, pp. 1089-1091, 2010.

[3] M.Akanegawa, Y.Tanaka and M.Nakagawa, “Basic study on traffic informarion system using LED traffic lights,” IEEE Trans. ITS., vol.2, No.4, pp.197-203, Dec., 2001.